UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,510	07/25/2003	Jeffrey V. Lindholm	X-1390 US	3272

24309 7590 02/21/2006

XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
DINH, PAUL	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/627,510	LINDHOLM ET AL.	
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Paul Dinh

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the remarks filed on 1/17/06. The remarks are not persuasive; therefore, the rejections based on the prior art of record **Agrawal** are maintained.

Claims 1-21 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Agrawal et al (US Patent Application No. 2004/0010767)

(Claims 1, 8, 15)

A common software tile comprising a description of the common routing resources

(I.e., see one or more of: processing/routing, place-and route software programmable routing resources, programmable routing switches, signal routing resources, switch matrix for routing, switch box for routing, switch block for routing and programmable interconnect points (PIP) in one or more of: para. 0010-0011, 0040-0041, 0059, 0098-0099, fig 1-5),

The common software tile having first terminals (first/second terminal in fig 2-4) for coupling an instance of the common software tile to other instances of the common software tile and further having second terminals (*see one or more of:* para 0011, 0015, 0038, 0040-0041, 0047, 0051, 0059, fig 4); and

For each hardware tile (hardware tiles in fig 2-4), a unique software tile comprising a description of the unique logic resources (logic resources = GLBs, CLBs, logic tiles one or more of: in fig 2-4. para 0072) included in the hardware tile, each unique software tile comprising terminals (terminals in fig 2-4) for coupling the unique software tile to the second terminals

(first/second terminal in fig 2-4) of an instance of the common software tile (para 0011, 0015, 0038, 0040-0041, 0047, 0051, 0059, fig 4)

(Claims 2, 9, 16) wherein each hardware tile further includes unique routing resources unique to each hardware tile (abstract, para 0011, 0015, 0038, 0040-0041, 0047, 0051, 0059, fig 2-4); and the unique software tile for each hardware tile further comprises a unique description of the unique routing resources included in the hardware tile (abstract, para 0011, 0015, 0038, 0040-0041, 0047, 0051, 0059, fig 2-4)

(Claims 3, 10, 17) wherein the PLD is a FPGA (abstract, summary, fig 1-4)

(Claims 4, 11, 18) wherein the plurality of programmable hardware tiles comprises at least one of the following types of logic blocks: configurable logic blocks (CLBs), Random Access Memory (RAM) blocks, multiplier blocks, and processor blocks (fig 1-4).

(Claims 5, 12, 19) wherein the plurality of programmable hardware tiles further comprises I/O blocks (para 0010, 0019, 0034, 0074, 0086, 0097, fig 1-4)

(Claims 6, 13, 20) further comprising a PLD device model representing a placement of the plurality of programmable hardware tiles in the PLD and comprising instances of the common software tile and the unique software tiles (para 0010, 0013, 0019, 0033, 0038, 0059-0061, 0090, 0099, fig 2-4), the PLD device model utilizing a uniform numbering scheme based on numbered instances of the common software tile (para 0010, 0013, 0019, 0033, 0038, 0059-0061, 0090, 0099, fig 2-4)

(Claims 7, 14, 21) wherein the plurality of programmable hardware tiles comprises an entirety of the programmable hardware tiles in the PLD (para 0010, 0013, 0019, 0033, 0038, 0059-0061, 0090, 0099, fig 2-4).

Response to Applicant Remarks

The prior art of record Agrawal discloses all the elements recited in the claims as detailed and explained above.

The applicants states: "As noted in Applicants' paragraph (0008), "the correspondence between hardware tiles and software tiles is maintained by known software representations, regardless of the hierarchical nature of the software tile." Agrawal does not teach or suggest any

other approach. It is note that the limitation that the applicants relies on, i.e., "the correspondence between hardware tiles and software tiles is maintained by known software representations, regardless of the hierarchical nature of the software tile." Is not recited in the claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Note that even though Agrawal does not use the terms "common" and "unique" in common software tile and unique software tile; the software (software tiles) of Agrawal (*I.e., see one or more of: processing/routing, place-and route software, programmable routing resources, programmable routing switches, signal routing resources, switch matrix for routing, switch box for routing, switch block for routing and programmable interconnect points (PIP) in one or more of: para. 0010-0011, 0040-0041, 0059, 0098-0099, fig 1-5*) are considered common and unique because Agrawal discloses all the elements recited in the claims as detailed and explained above. The software (software tiles) of Agrawal represents/used for routing/interconnecting hardware devices (i.e., PLD/FPGA, CLBs, GLBs, functional circuits, logic gates, tiles, tile model/programmable, etc, as shown in fig 2-5).

Regarding the remarks that "the reference does not contain any references to software tiles, device modeling, modeling software, software representations of PLDS, and so forth, which is the subject matter of the present claims"; Agrawal clearly discloses software tiles, device modeling, modeling software, software representations of PLDS; i.e.,

See one or more of:

Place-and route software, programmable routing resources, programmable routing switches, signal routing resources, switch matrix for routing, switch box for routing, switch block for routing and programmable interconnect points (PIP) in one or more of: para. 0010-0011, 0040-0041, 0059, 0098-0099, fig 1-5; and

Device model 100 in fig 1-2, device model, tile model in fig 4-5; and

PPGA implemented by programming/software, software representation of PLD in para 0059-0061, and fig 1-5; and

Tiles programmable in fig 4; and

Place-and route software for tiles in para 0090; and

Instructions to computers for causing the computers to perform automated place-and-route operations for the automated generation of FPGA configuration in para 0106, etc.

The request that the next office action be a non-final office action is not granted because the prior art of record discloses all the elements recited in the claims as detailed and explained above.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Dinh
Primary Examiner